

Figure 4 - Limiting at 0.5V and 4.5V

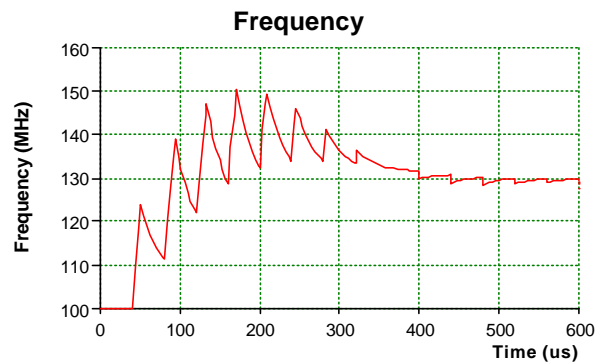


Figure 5 - Expanded transient, no saturation

To summarize:

| Clipping Level (Volts) | Time to Lock to 1kHz (ms) |
|------------------------|---------------------------|
| None | 1.21 |
| 5 | 1.38 |
| 4.5 | 1.69 |
| 4.25 | 2.21 |

Note that in each case the target steady state voltage on the VCO control line is 4V.

So it can be seen that failing to provide adequate headroom in the charge pump output can lead to significant increases in PLL lock times. It also indicates that normal production variations in VCO tuning law can lead to significant variations in PLL lock time.

Discussion of Effect

The reason for this effect may be readily understood from the loop filter schematic Figure 1 and the unclipped transient in Figure 2. Expanding the early part of the transient we see

In the loop filter in Figure 1,

$$C_1 \approx 0.1C_2$$

At the beginning of the transient, the charge pump supplies current to the loop filter to increase the VCO voltage. During the short phase detector pulses this current flows primarily into C_1 , (the voltage spikes) and in-between the spikes much of the charge from C_1 flows through R_1 to C_2 (the decaying voltage between the spikes). To get a reasonable current flow into C_2 (which is the biggest) necessarily requires the voltage across C_1 to rise to levels significantly above the voltage across C_2 . Limiting these spikes significantly reduces the flow of current into C_2 .

Conclusion

The voltage headroom provided at by the charge pump phase detector can have significant effect on PLL lock time. The lack of sufficient headroom can result in a major degradation of locking performance.

The effect on lock times can be readily determined using a simulation package such as SimPLL.

REFERENCES:

1. SimPLL software package, available at: www.radiolab.com.au (note all simulations in this article can be performed using the free demo version of SimPLL)

For further information visit www.radiolab.com.au,